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Description:

The Communications/Memory Module is an expansion daughtercard for use with the Avalon Reference Design System™. The daughtercard interfaces via AvBus connectors and provides general-purpose resources to complement Avalon base modules. The daughtercard provides all necessary resources for implementation of Xilinx™ MicroBlaze™ core designs.

Ordering Information:

The following table lists the Module part numbers and available software options.

Internet Link at <http://www.em.avnet.com/>

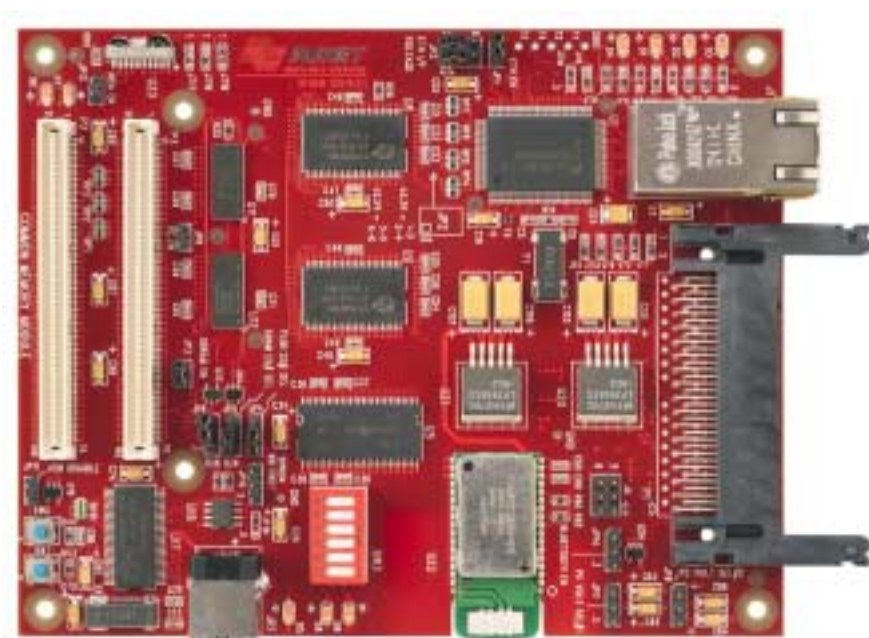
| Part Number | Description |
|----------------|---|
| ADS-EMU-DAU | Communications/Memory Module |
| ADS-XLX-MB-DAU | Communications/Memory Module bundled with MicroBlaze Core License |

Features:

- ▲ 64 Mbytes SDRAM
- ▲ 16 Mbytes FLASH
- ▲ 1 Mbyte SRAM
- ▲ 10/100/1000 Ethernet PHY
- ▲ Blue Tooth Module
- ▲ IrDA
- ▲ USB 2.0
- ▲ PC Card

Target Applications:

- ▲ Complete resources for implementation of Xilinx MicroBlaze Core
- ▲ Functional expansion of Avalon Reference Design System evaluation and development kits
- ▲ Ethernet 10/100/1000 interface
- ▲ PC Card development
- ▲ USB 2.0 applications



1.0 Overview

The Communications/Memory Module is a daughterboard, which provides additional memory resources and communications capabilities to motherboards, which are compliant with the Avnet Design Services Avalon Reference Design System™. In particular, this module will focus on providing the memory subsystems needed for demonstration of the Xilinx Platform FPGAs with embedded hard (IBM PowerPC™) and soft (MicroBlaze™) processor cores and a peripheral set which demonstrates the versatility of the Xilinx FPGA families. The module provides the following resources:

- 64 Mbytes SDRAM
- 16 Mbytes FLASH
- 1 Mbyte SRAM
- 10/100/1000 Ethernet PHY
- Bluetooth Serial Module
- IrDA
- USB 2.0
- PC Card

2.0 Capabilities Matrix

While the Communications/Memory Module is intended to be used by any motherboard compliant with the Avalon Reference Design System™, the design has been optimized for the Avnet Xilinx Virtex-II Pro Evaluation board, the Avnet Xilinx™ Virtex-II Development board, the Avnet Xilinx Spartan®-IIE Evaluation board, and the Avnet Xilinx Virtex-E Development board. Various combinations of resources are available depending on which board the module is supporting, the FPGA installed on the motherboard and how it is attached.

The Communications/Memory Module can be connected to the Virtex-II Development board, the Spartan-IIE Evaluation board or the Virtex-E Development board in two ways. The first, the normal connection, has both AvBus connectors on the motherboard connected with both AvBus connectors on the module. The other method, the offset connection, has only one of the AvBus connectors used on each board.

Normal (2 connector)

Xilinx Virtex-II Pro Evaluation Board P2 to Communications/Memory Module J2
Xilinx Virtex-II Pro Evaluation Board P1 to Communications/Memory Module J3

Xilinx Virtex-II Development Board P5 to Communications/Memory Module J2
Xilinx Virtex-II Development Board P4 to Communications/Memory Module J3

Xilinx Spartan-IIE Evaluation Board P2 to Communications/Memory Module J2
Xilinx Spartan-IIE Evaluation Board P1 to Communications/Memory Module J3

Xilinx Virtex-E Development Board P12 to Communications/Memory Module J2
Xilinx Virtex-E Development Board P11 to Communications/Memory Module J3

***Offset (1 connector)**

Xilinx Virtex-II Development Board P4 to Communications/Memory Module J2
Xilinx Virtex-II Development Board P5 No Connect
Communications/Memory Module J3 No Connect

Xilinx Spartan-IIE Evaluation Board P1 to Communications/Memory Module J2
Xilinx Spartan-IIE Evaluation Board P2 No Connect
Communications/Memory Module J3 No Connect

Xilinx Virtex-E Development Board P11 to Communications/Memory Module J2
Xilinx Virtex-E Development Board P12 No Connect

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Communications/Memory Module J3 No Connect

*Top vs. Bottom Mount

It should be noted that Evaluation boards are equipped with Avbus connectors on both sides of the PCB. Since the connectors on the solder side are in parallel with their component-side counterparts, and the Comm/Memory module is similarly equipped, the boards may be stacked with either on top. Moving the module board to the bottom may give access (probing, visibility, etc...) to components which were otherwise inaccessible in a Top mount configuration. Development boards are not equipped with these mirrored Avbus connectors thus a Top mount configuration must be used.

*The user should always exercise caution when connecting boards in alternate configurations to ensure that no physical interferences are created.

The Xilinx Virtex-II Development Board can be assembled with either an XC2V1500, XC2V2000 in the FF856 package, or an XC2V4000-10000 in the FF1152 package.

The table below shows the combinations of part type and connection versus the resources available to the motherboard from the Communications/Memory Module.

| | SDRAM | SRAM | Flash | GbE | IrDA | USB | PCCard | Notes |
|--|-------|------|-------|-----|------|-----|--------|-------|
| Xilinx Virtex-II Pro Evaluation Board 2VP7, FF896, Normal | X | X | X | X | X | X | X | |
| Xilinx Virtex-II Development Board 1500, FF896, Normal | X | X | X | X | X | | | |
| Xilinx Virtex-II Development Board 1500, FF896, Offset | | | | X | X | X | X | |
| Xilinx Virtex-II Development Board 2000, FF896, Normal | X | X | X | X | X | | X | |
| Xilinx Virtex-II Development Board 2000, FF896, Offset | | | | X | X | X | X | |
| Xilinx Virtex-II Development Board 4000+, FF1152, Normal | X | X | X | X | X | X | X | |
| Xilinx Virtex-II Development Board 4000+, FF1152, Offset | | | | X | X | X | X | |
| Xilinx Spartan-II Evaluation Board Normal | X | X | X | X | X | | | |
| Xilinx Spartan-II Evaluation Board Offset | | | | X | X | X | | |
| Xilinx Virtex-E Development Board Normal | X | X | X | X | X | | X | |
| Xilinx Virtex-E Development Board Offset | | | | X | X | X | X | |

Table 2-1: Capabilities Matrix

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3.0 Block Diagram

The following diagram displays the hardware for Communications/Memory Module.

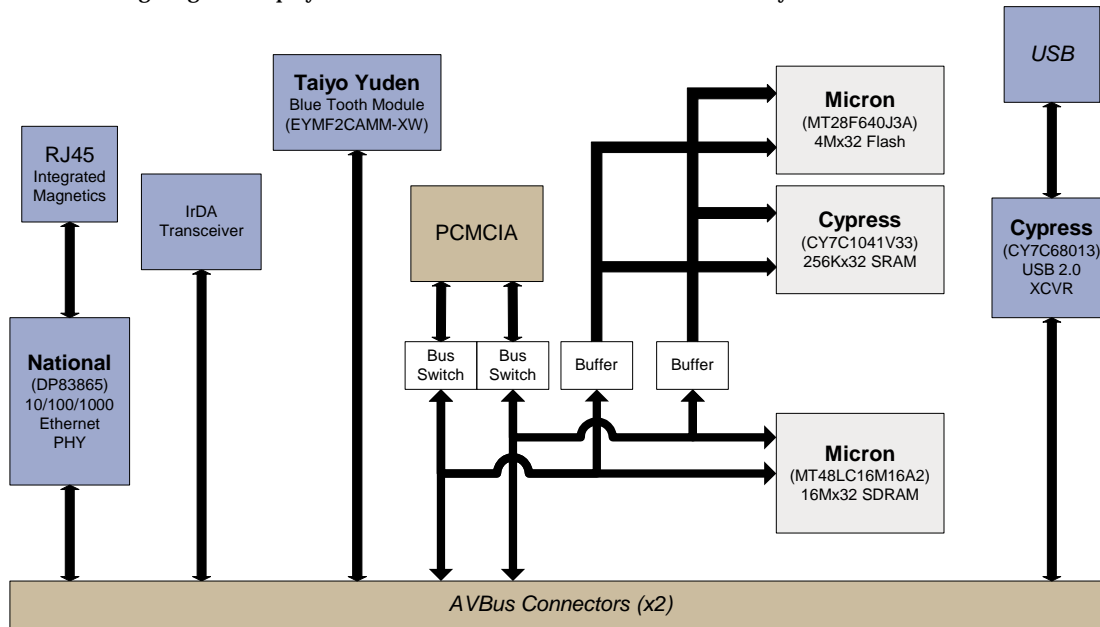


Figure 1: Communications/Memory Module Block Diagram

4.0 Mechanical

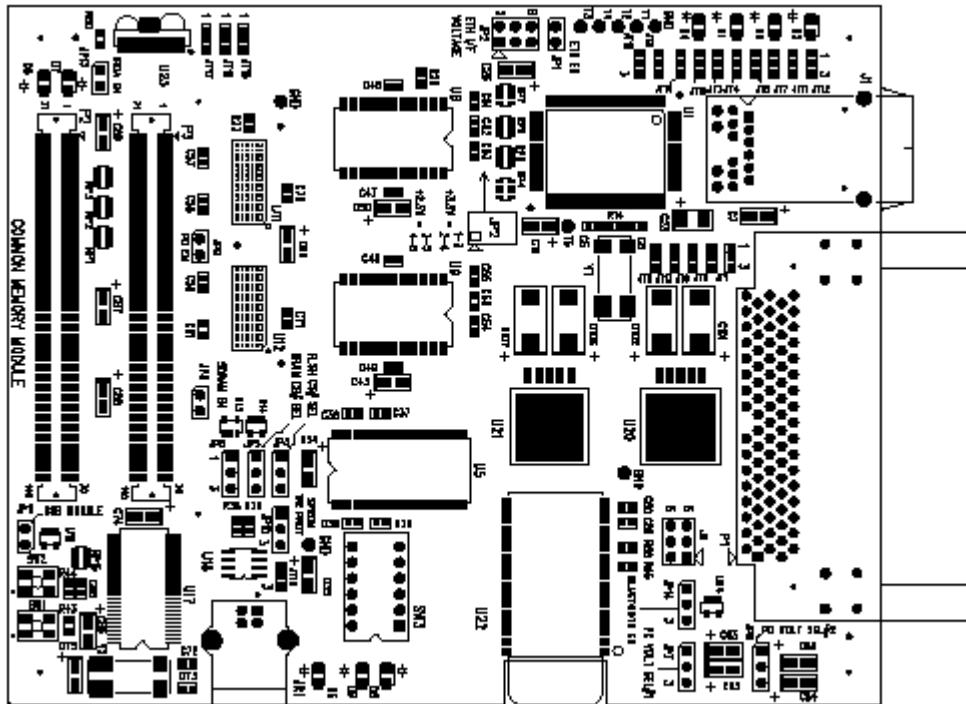


Figure 2: Part Placement – Top

Board Dimensions: 5.5" x 4.4"

The Communications/Memory Module Printed Circuit Board (PCB) is an eight-layer board, which has three signal layers, two ground planes and a +3.3V power plane. The board stack-up is as follows:

- Layer 1: Primary Component
- Layer 2: Ground Plane
- Layer 3: Signal
- Layer 4: Signal
- Layer 5: Ground
- Layer 6: Signal
- Layer 7: +3.3VDC Power
- Layer 8: Secondary Component

5.0 User Information

5.1 Power

Power is applied to the Communication/Memory Daughter card from a host board through the AvBus connectors.

5.2 Jumper Settings

Jumpers are provided on this board to allow the user to enable/disable each peripheral independently of the others to allow the signals connected to unused peripherals to be used for alternate purposes. By default all peripheral are enabled at the factory.

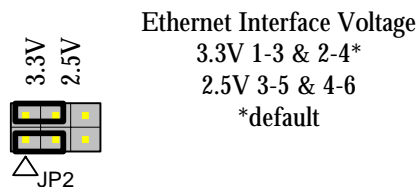
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JP1 Ethernet Enable

When jumper is open a pull down resistor (R16) holds the DP83865 Ethernet Phy in Reset. Installing a shunt at this position connects the Phy reset pin to the associated pin on the AvBus connector enabling it to be controlled by a host FPGA/Controller.

JP2 Ethernet Phy Interface Voltage

The DP83865 Phy is capable of interfacing to 2.5V and 3.3V MACs if properly configured by this jumper. Both shunts must be moved together for proper Phy operation. Review the National Semiconductor DP83865 data sheet for more information.



JP3 SDRAM Enable

When this jumper is open a pull up resistor (R27) holds the SDRAM chip select high disabling the device. Installing a shunt at this position connects the SDRAM chip select pin to the associated pin on the AvBus connector enabling it to be asserted by a host FPGA/Controller.

JP4 FLASH CS# select

This three way jump is used to enable the FLASH devices and to select between two possible AvBus interface pins to avoid conflicts with memories on the host board. When the shunt is removed the CS# pin of the FLASH devices is pulled high by a resistor (R35), deservting the pin and thus disabling the device. When a shunt is placed between pins 1 and 2 the FLASH chip select net is controlled by pin 119 of the AvBus connectors (P3 and/or J3). When a shunt is placed between pins 2 and 3 the FLASH chip select net is controlled by pin 63 of the AvBus connectors (P3 and/or J3).

JP5 SRAM CS# select

This three way jump is used to enable the SRAM devices and to select between two possible AvBus interface pins to avoid conflicts with memories on the host board. When the shunt is removed the CS# pin of the SRAM devices is pulled high by a resistor (R34), deservting the pin and thus disabling the device. When a shunt is placed between pins 1 and 2 the SRAM chip select net is controlled by pin 124 of the AvBus connectors (P3 and/or J3). When a shunt is placed between pins 2 and 3 the SRAM chip select net is controlled by pin 50 of the AvBus connectors (P3 and/or J3).

JP6 Buffer Enable

When a shunt is placed between pins 1 and 2 the output enable of the static memory data buffers is decoded from the FLASH and SRAM chip select signals. For applications that don't require any static memory the shunt can be moved to short pins 2 and 3 deservting the buffer.

JP7 and JP8 PC-Card Voltage select

These jumpers are used to select the power supplies to be connected to Vcc and Vpp of the PC-Card socket. Before installing a card in the provided slot you must review the requirements of the card and the schematic to insure proper settings.

JP9 PC-Card Enable

When this jumper is open a pull up resistor (R36) deserts the output enable signal of the bus switches between the AvBus connector and the PC-Card socket tri-stating the associated signals. Applying a shunt to this jumper ties the output enable to ground enabling the interface.

JP10 EEPROM Write Protect

Placing a shunt between pins 1 and 2 places the serial EEPROM (U18) in read/write mode allowing the user to update the configuration of the CY7C68013 USB 2.0 controller. Moving the shunt to cover pins 2 and 3 puts the EEPROM in read only mode, protecting its contents from being corrupted.

JP11 USB Reset

Placing a shunt on JP11 forces the CY7C68013 USB 2.0 controller into reset allowing the interface pins to be used for alternate functions.

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JP12 Blue Tooth Enable

This three pin jumper enables the user to force the Blue Tooth Module into the reset state (1-2) or to allow the host board to control its reset (2-3) via the RST# signal. With the shunt removed completely the USB reset signal is held deserted by a pull down resistor (R63).

JP13 IRDA RXD

The HSDL3602-007 IRDA transceiver has only one output, RXD. With a shunt installed on JP13 the RXD signal is connected to the AvBus connector to allow IRDA communication. With the shunt removed the Net is broken allowing the I/O to be used for alternate functions.

6.0 Memory Interfaces

6.1 AvBus

The memory is interfaced to the Communication/Memory module is provided to the host board via the mirrored AvBus connectors P3 and J3. This connector pair provides 32 bits of address bus, 32 bits of data bus and the required memory control signals. To reduce bus loading only the SDRAM is connected directly to the AvBus connector. All SRAM and FLASH signals and control are buffered. This bus is also multiplexed with the PC-Card connector, which is separated from the AvBus by CBT bus switches to allow bi-directional data on all signals.

6.2 SDRAM

Two Micron MT48LC16M16A2 256Mbit SDRAM devices are used to provide 64Mbytes of SDRAM organized as 16M x 32. The board was designed to support SDRAM clock rates over 100MHz but the actual performance is not guaranteed because it is reliant on customer developed hardware and logic.

6.3 SRAM

Two 256K x 16 SRAM devices are used to provide 1Mbytes of SRAM organized as 256K x 32. The SRAM components will be 15nS or faster but remember to add ~5nS to the timing budget for the signals to propagate through the buffers. See the description of the jumper "JP5" for chip select information.

6.4 FLASH

Two Micron 28F640J FLASH devices are used to provide a 16 Mbytes of memory organized as 4M x 32. Extra address pins are available to allow the user to double the size of the FLASH by replacing the components with 28F128J (128Mbit) devices. Sockets are not provided for these devices so the host board must perform programming sequences. See the description of the jumper "JP4" for chip select information.

7.0 Communication Interfaces

The Communications/Memory Module provides several interfaces:

- Gigabit Ethernet
- IrDA
- PCMCIA/PCCard
- USB 2.0
- Blue Tooth

7.1 Ethernet PHY

The PHY is a National DP83865BVH Gig PHYTER® V. The DP83865 is a low power version of National's Gig PHYTER V with a 1.8V core voltage and 2.5V or 3.3V I/O voltage. The PHY is connected to a Pulse RJ-45 jack with integrated magnetics (part number: JK0654218Z). The jack also integrates two LEDs to show Link and Activity. External logic was used to logically OR the three link indicators for 10, 100 and 1000 Mb/s to drive the Link LED on the RJ-45 jack. The external logic is for the default strap options and may not work if the strap options are changed. Four more LEDs are provided on the board for status indication. These LEDs indicate Link at 10 Mb/s, Link at 100 Mb/s, Link at 1000 Mb/s and Full Duplex operation. The PHY clock is generated from its own 25 MHz crystal. The PHY address is set to 0b10001 by default. Three-pad resistor jumpers were used to set the strapping options. These jumper pads provide the user with the ability to change the settings by moving the resistors. The strapping options are shown in the table below. The dual-function pins that are used for a strapping option and to drive an LED, have a set of two jumpers per pin. An asterisk in the Table 10 below indicates the dual-function pins.

| Function | Jumper Installation | Resistor | Mode Enabled |
|-------------------------|---------------------|----------|---|
| Auto-Negotiation* | JT3: pins 1-2 | 0 ohm | Auto-negotiation enabled (default) |
| | JT4: pins 2-3 | 0 ohm | |
| | JT3: pins 2-3 | 0 ohm | Auto-negotiation disabled |
| | JT4: pins 1-2 | 0 ohm | |
| Full/Half Duplex* | JT6: pins 1-2 | 0 ohm | Full Duplex (default) |
| | JT7: pins 2-3 | 0 ohm | |
| | JT6: pins 2-3 | 0 ohm | Half Duplex |
| | JT7: pins 1-2 | 0 ohm | |
| Speed 1* | JT11: pins 2-3 | 0 ohm | Speed Selection: (Auto-Neg enabled) <u>Speed1</u> <u>Speed0</u> <u>Speed Advertised</u> 1 1 1000BASE-T, 10BASE-T 1 0 1000BASE-T 0 1 1000BASE-T, 100BASE-TX 0 0 1000BASE-T, 100BASE-TX, 10BASE-T Default: 1000BASE-T, 100BASE-TX, 10BASE-T |
| | JT12: pins 1-2 | 0 ohm | |
| | (Speed1 – 0) | | |
| | | | |
| Speed 0* | JT1: pins 2-3 | 0 ohm | |
| | JT2: pins 1-2 | 0 ohm | |
| | (Speed0 – 0) | | |
| | | | |
| PHY address 0* | JT14: pins 1-2 | 0 ohm | PHY Address 0b10001 (default) |
| | JT15: pins 2-3 | 0 ohm | |
| | JT14: pins 2-3 | 0 ohm | PHY Address 0b10000 |
| | JT15: pins 1-2 | 0 ohm | |
| Non-IEEE Compliant Mode | JT8: pins 2-3 | 1 K | Compliant and Non-comp. Operation (default) |
| | JT8: pins 1-2 | 1 K | Inhibits Non-compliant operation |
| Manual MDIX Setting | JT10: pins 1-2 | 1 K | Straight Mode (default) |
| | JT10 pins 2-3 | 1 K | Cross-over Mode |
| Auto MDIX Enable | JT13: pins 2-3 | 1 K | Automatic Pair Swap – MDIX (default) |
| | JT13: pins 1-2 | 1 K | Set to manual preset – Manual MDIX Setting (JT12) |
| Multiple Node Enable | JT9: pins 1-2 | 1 K | Single node – NIC (default) |
| | JT9: pins 2-3 | 1 K | Multiple node priority – switch/hub |
| Clock to MAC Enable | JT5: pins 1-2 | 1 K | CLK_TO_MAC output disabled (default) |
| | JT5: pins 2-3 | 1 K | CLK_TO_MAC output enabled |

Table 7-1 - Ethernet PHY Strapping Options

The default options as indicated in Table 10 are Auto-Negotiation enabled, Full Duplex mode, Speed advertised as 10/100/1000 Mb/s, PHY address 0b10001, IEEE Compliant and Non-compliant support, straight cable in non-MDIX mode, auto-MDIX mode enabled, Single node (NIC) and CLK_TO_MAC disabled. The pin-out for a jumper pad is shown below.

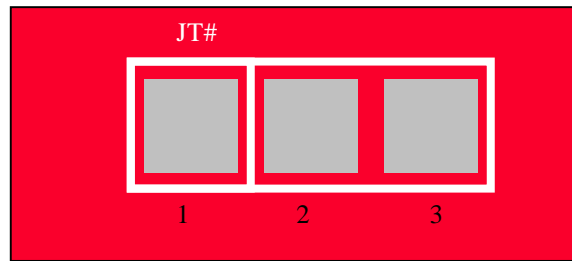


Figure 3 – Jumper Pad Pin-out

The auto-MDIX mode provides automatic swapping of the differential pairs. This allows the PHY to work with either a straight-through cable or crossover cable. Use a CAT-5e or CAT-6 Ethernet cable when operating at 1000 Mb/s (Gigabit Ethernet). The boundary-scan Test Access Port (TAP) controller of the PHY is not implemented in this design so a resistor (R15) is used to hold it in reset, allowing normal operation of the PHY.

7.2 IrDA

An Agilent HSDL-3602-007 IrDA transceiver is included on the board. This transceiver provides IrDA 1.1 compliant links from 9.6 kbps to 4Mbps. It is connected to the FPGA via the AvBus connector (J4, P4).

The configuration pins, Mode 0, Mode 1 and FIR Select pins of the transceiver are set using 4.7 K ohm resistor jumpers as follows:

| JT17 | JT18 | JT19 | Function |
|------|------|------|----------------------|
| 1-2 | | | FIR Select = SIR |
| 2-3 | | | FIR Select = MIR/FIR |
| | 1-2 | | Mode 1 = 0 |
| | 2-3 | | Mode 1 = 1 |
| | | 1-2 | Mode 0 = 0 |
| | | 2-3 | Mode 0 = 1 |

Table 7-2: IrDA Mode Select Settings

7.3 PCMCIA/PCCard

A PC Card connector is incorporated on the board and connected to the FPGA via the AvBus connector (J2, P2). The PC Card connector (P1) supports 26 address lines and 16 data lines. These address and data lines are buffered separately from the memory address and data busses (U12, U13). The socket does not support hot swapping. The Vcc and Vpp pins are selectable via jumpers (JP4, JP5) between +3.3 Vdc and +5 Vdc.

7.4 USB

A Cypress CY7C68013 single chip USB 2.0 full/high speed peripheral controller is incorporated on the board. This controller supports data transfers at Full Speed (12 Mbps) and High Speed (480 Mbps). The part is connected to a USB Type B connector (JR1). Though the USB circuit is powered by the +3.3V power plane of the board an LED (D5) indicates that the downstream device has recognized the connection and turned on the port power. Two pushbutton switches are included on the board to generate Reset (SW2) and Wakeup (SW1). The data path and control interfaces are connected to the FPGA via the AvBus connector (J2, P2).

The CY7C68013 is a programmable controller that will require additional user code to operate in most applications.

7.5 Blue Tooth

The EYMF2CAMP-XW integrated Blue Tooth Module from Taiyo Yuden is optionally included on the board allowing the user to create a wireless serial link to a peer or host device. The module comes preprogrammed from Taiyo Yuden but the SPI port is

brought out to the header “J6” to allow user access to reprogram the module if needed. The jumper JP14 is used to enable/disable the module (see above)

Switch settings for Blue Tooth operating modes.

| 1 | 2 | 3 | 4 | 5 | 6 | Function |
|---|----------------|----------------|------|---|---|------------------|
| OFF | Message Enable | | | | | Message Disabled |
| ON | | | | | | Message Enabled |
| | OFF | Operation Mode | | | | Automatic |
| | ON | | | | | Command Control |
| | | OFF | Role | | | Master |
| | | ON | | | | Slave |
| BAUD RATE Switch SW3-4, SW3-5 and SW3-6 are used to set the baud rate of the link. “0”= ON, “1”=OFF | | | 0 | 0 | 0 | 9600 |
| | | | 0 | 0 | 1 | 19200 |
| | | | 0 | 1 | 0 | 38400 |
| | | | 0 | 1 | 1 | 57600 |
| | | | 1 | 0 | 0 | 115200 |
| | | | 1 | 0 | 1 | 230400 |
| | | | 1 | 1 | 0 | 460800 |
| | | | 1 | 1 | 1 | 921600 |

Table 7-3: Blue Tooth Switch Settings

8.0 Connectors

8.1 AvBus

Avnet Design Services has defined four configurations for the AvBus connector. Two of those configurations are used in the Communication/Memory Module; AvBus Memory with JTAG and AvBus Memory without JTAG. The pin definitions for these connectors on the Communications/Memory Module are as follows:

| Pin | AvBus Spec Signal Name | Function | | Pin | AvBus Spec Signal Name | Function |
|-----|------------------------|----------|--|-----|------------------------|----------|
| | | | | | | |
| 1 | +5Vdc | | | 71 | Addr0 | A0 |
| 2 | Addr1 | A1 | | 72 | Gnd | |
| 3 | Addr2 | A2 | | 73 | Addr3 | A3 |
| 4 | Gnd | | | 74 | Addr4 | A4 |
| 5 | Addr5 | A5 | | 75 | Gnd | |
| 6 | Addr6 | A6 | | 76 | Addr7 | A7 |
| 7 | Gnd | | | 77 | Addr8 | A8 |
| 8 | Addr9 | A9 | | 78 | +3.3Vdc | |
| 9 | Addr10 | A10 | | 79 | Addr11 | A11 |
| 10 | Gnd | | | 80 | Addr12 | A12 |
| 11 | Addr13 | A13 | | 81 | Gnd | |
| 12 | Addr14 | A14 | | 82 | Addr15 | A15 |
| 13 | +5Vdc | | | 83 | Addr16 | A16 |
| 14 | Addr17 | A17 | | 84 | Gnd | |
| 15 | Addr18 | A18 | | 85 | Addr19 | A19 |
| 16 | Gnd | | | 86 | Addr20 | A20 |
| 17 | Addr21 | A21 | | 87 | Gnd | |
| 18 | Addr22 | A22 | | 88 | Addr23 | A23 |
| 19 | Gnd | | | 89 | Addr24 | A24 |

| Pin | AvBus Spec Signal Name | Function | | Pin | AvBus Spec Signal Name | Function |
|-----|------------------------|--------------|--|-----|------------------------|--------------|
| 20 | Addr25 | A25 | | 90 | +3.3Vdc | |
| 21 | Addr26 | A26 | | 91 | Addr27 | A27 |
| 22 | Gnd | | | 92 | Addr28 | A28 |
| 23 | Addr29 | A29 | | 93 | Gnd | |
| 24 | Addr30 | A29 | | 94 | Addr31 | A31 |
| 25 | +5Vdc | | | 95 | Data0 | D0 |
| 26 | Data1 | D1 | | 96 | Gnd | |
| 27 | Data2 | D2 | | 97 | Data3 | D3 |
| 28 | Gnd | | | 98 | Data4 | D4 |
| 29 | Data5 | D5 | | 99 | Gnd | |
| 30 | Data6 | D6 | | 100 | Data7 | D7 |
| 31 | Gnd | | | 101 | Data8 | D8 |
| 32 | Data9 | D9 | | 102 | +3.3Vdc | |
| 33 | Data10 | D10 | | 103 | Data11 | D11 |
| 34 | Gnd | | | 104 | Data12 | D12 |
| 35 | Data13 | D13 | | 105 | Gnd | |
| 36 | Data14 | D14 | | 106 | Data15 | D15 |
| 37 | +5Vdc | | | 107 | Data16 | D16 |
| 38 | Data17 | D17 | | 108 | Gnd | |
| 39 | Data18 | D18 | | 109 | Data19 | D19 |
| 40 | Gnd | | | 110 | Data20 | D20 |
| 41 | Data21 | D21 | | 111 | Gnd | |
| 42 | Data22 | D22 | | 112 | Data23 | D23 |
| 43 | Gnd | | | 113 | Data24 | D24 |
| 44 | Data25 | D25 | | 114 | +3.3Vdc | |
| 45 | Data26 | D26 | | 115 | Data27 | D27 |
| 46 | Gnd | | | 116 | Data28 | D28 |
| 47 | Data29 | D29 | | 117 | Gnd | |
| 48 | Data30 | D30 | | 118 | Data31 | D31 |
| 49 | +5Vdc | | | 119 | Flash_CE0# | FL_CS#_119 |
| 50 | Flash_CE1# | SRAM_CS#_50 | | 120 | Gnd | |
| 51 | Flash_OE# | OE# | | 121 | Flash_WE# | WE# |
| 52 | Gnd | | | 122 | Flash_Reset# | RST# |
| 53 | SDRAM_CS# | SDRAM_CS# | | 123 | Gnd | |
| 54 | SDRAM_CAS# | CAS# | | 124 | SDRAM_WE# | SRAM_CS#_124 |
| 55 | Gnd | | | 125 | SDRAM_Clk | CLK |
| 56 | SDRAM_RAS# | RAS# | | 126 | +3.3Vdc | |
| 57 | SDRAM_ClkEn | CLKEN | | 127 | SDRAM_Byte0# | BS0# |
| 58 | Gnd | | | 128 | SDRAM_Byte1# | BS1# |
| 59 | SDRAM_Byte2# | BS2# | | 129 | Gnd | |
| 60 | SDRAM_Byte3# | BS3# | | 130 | User_I/O0 | IRDA_TXD |
| 61 | +5Vdc | | | 131 | User_I/O1 | IRDA_RXD |
| 62 | User_I/O2 | IRDA_FIR_SEL | | 132 | Gnd | |
| 63 | User_I/O3 | FL_CS#_63 | | 133 | User_I/O4 | N/C |
| 64 | Gnd | | | 134 | User_I/O5 | N/C |
| 65 | User_I/O6 | N/C | | 135 | Gnd | |
| 66 | User_I/O7 | N/C | | 136 | User_I/O8 | N/C |
| 67 | Gnd | | | 137 | TMS | TMS |
| 68 | TDO | TDO | | 138 | +3.3Vdc | |
| 69 | TCK | TCK | | 139 | TDI | TDI |
| 70 | Gnd | | | 140 | TRST | TRST# |

Table 8-1: AvBus Memory Connector (with JTAG)

| Pin | AvBus Spec Signal Name | Function | | Pin | AvBus Spec Signal Name | Function |
|-----|------------------------|----------|--|-----|------------------------|----------|
| | | | | | | |
| 1 | +5Vdc | | | 71 | Data32 | GMII_MDC |

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| Pin | AvBus Spec Signal Name | Function | Pin | AvBus Spec Signal Name | Function |
|-----|------------------------|-------------|-----|------------------------|--------------|
| 2 | Data33 | GMII_MDIO | 72 | Gnd | |
| 3 | Data34 | GMII_COL | 73 | Data35 | GMII_CRS |
| 4 | Gnd | | 74 | Data36 | GMII_RXD7 |
| 5 | Data37 | GMII_RX_ER | 75 | Gnd | |
| 6 | Data38 | GMII_RX_CLK | 76 | Data39 | GMII_RX_DV |
| 7 | Gnd | | 77 | Data40 | GMII_RXD6 |
| 8 | Data41 | GMII_RXD5 | 78 | +3.3Vdc | |
| 9 | Data42 | GMII_RXD3 | 79 | Data43 | GMII_RXD4 |
| 10 | Gnd | | 80 | Data44 | GMII_RXD2 |
| 11 | Data45 | GMII_RXD1 | 81 | Gnd | |
| 12 | Data46 | GMII_TX_CLK | 82 | Data47 | GMII_RXD0 |
| 13 | +5Vdc | | 83 | Data48 | GMII_TX_ER |
| 14 | Data49 | GMII_TX_EN | 84 | Gnd | |
| 15 | Data50 | GMII_TXD6 | 85 | Data51 | GMII_TXD7 |
| 16 | Gnd | | 86 | Data52 | GMII_TXD5 |
| 17 | Data53 | GMII_TXD4 | 87 | Gnd | |
| 18 | Data54 | GMII_TXD2 | 88 | Data55 | GMII_TXD3 |
| 19 | Gnd | | 89 | Data56 | GMII_GTC_CLK |
| 20 | Data57 | GMII_TXD0 | 90 | +3.3Vdc | |
| 21 | Data58 | GMII_TXD1 | 91 | Data59 | GBEINT# |
| 22 | Gnd | | 92 | Data60 | GBE_RST# |
| 23 | Data61 | IRDA_MD0 | 93 | Gnd | |
| 24 | Data62 | IRDA_MD1 | 94 | Data63 | N/C |
| 25 | +5Vdc | | 95 | Flash_CE2# | PCC_REG# |
| 26 | Flash_CE3# | BT_RTS | 96 | Gnd | |
| 27 | SDRAM_Byte4# | BT_CTS | 97 | SDRAM_Byte5# | USB_INT0# |
| 28 | Gnd | | 98 | SDRAM_Byte6# | USB_INT1# |
| 29 | SDRAM_Byte7# | BT_TX | 99 | Gnd | |
| 30 | User_I/O0 | BT_RX | 100 | User_I/O1 | PCC_IORD# |
| 31 | Gnd | | 101 | User_I/O2 | PCC_IOWR# |
| 32 | User_I/O3 | PCC_CE2# | 102 | +3.3Vdc | |
| 33 | User_I/O4 | PCC_CE1# | 103 | User_I/O5 | PCC_WP |
| 34 | Gnd | | 104 | User_I/O6 | PCC_WAIT# |
| 35 | User_I/O7 | USB_FD1 | 105 | Gnd | |
| 36 | User_I/O8 | USB_FD2 | 106 | User_I/O9 | PCC_CD1# |
| 37 | +5Vdc | | 107 | User_I/O10 | PCC_CD2# |
| 38 | User_I/O11 | USB_FD3 | 108 | Gnd | |
| 39 | User_I/O12 | USB_FD4 | 109 | User_I/O13 | PCC_RDY_BSY |
| 40 | Gnd | | 110 | User_I/O14 | PCC_INPACK# |
| 41 | User_I/O15 | USB_FD5 | 111 | Gnd | |
| 42 | User_I/O16 | USB_FD6 | 112 | User_I/O17 | PCC_BVD2 |
| 43 | Gnd | | 113 | User_I/O18 | PCC_BVD1 |
| 44 | User_I/O19 | USB_FD7 | 114 | +3.3Vdc | |
| 45 | User_I/O20 | USB_FD8 | 115 | User_I/O21 | PCC_VS1 |
| 46 | Gnd | | 116 | User_I/O22 | PCC_VS2 |
| 47 | User_I/O23 | USB_FD9 | 117 | Gnd | |
| 48 | User_I/O24 | USB_FD10 | 118 | User_I/O25 | USB_IFCLK |
| 49 | +5Vdc | | 119 | User_I/O26 | USB_CLKOUT |
| 50 | User_I/O27 | USB_FD11 | 120 | Gnd | |
| 51 | User_I/O28 | USB_FD12 | 121 | User_I/O29 | USB_SLCS# |
| 52 | Gnd | | 122 | User_I/O30 | USB_PEND |
| 53 | User_I/O31 | USB_FD13 | 123 | Gnd | |
| 54 | User_I/O32 | USB_FD14 | 124 | User_I/O33 | USB_FA0 |
| 55 | Gnd | | 125 | User_I/O34 | USB_FA1 |
| 56 | User_I/O35 | USB_FD15 | 126 | +3.3Vdc | |
| 57 | User_I/O46 | USB_RDY0 | 127 | User_I/O37 | USB_FD0 |
| 58 | Gnd | | 128 | User_I/O38 | USB_SLOE |
| 59 | User_I/O39 | USB_RDY1 | 129 | Gnd | |
| 60 | User_I/O40 | USB_CTL0 | 130 | User_I/O41 | USB_WU2 |

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| Pin | AvBus Spec Signal Name | Function | Pin | AvBus Spec Signal Name | Function |
|-----|------------------------|----------|-----|------------------------|----------|
| 61 | +5Vdc | | 131 | User_I/O42 | USB_CTL2 |
| 62 | User_I/O43 | USB_CTL1 | 132 | Gnd | |
| 63 | User_I/O44 | N/C | 133 | User_I/O45 | N/C |
| 64 | Gnd | | 134 | User_I/O46 | N/C |
| 65 | User_I/O47 | N/C | 135 | Gnd | |
| 66 | User_I/O48 | N/C | 136 | User_I/O49 | N/C |
| 67 | Gnd | | 137 | User_I/O50 | N/C |
| 68 | User_I/O51 | N/C | 138 | +3.3Vdc | |
| 69 | User_I/O52 | N/C | 139 | User_I/O53 | N/C |
| 70 | Gnd | | 140 | User_I/O54 | N/C |

Table 8-2: AvBus Memory Connector (No JTAG)

8.2 USB Type B

| Pin | Definition |
|-----|-------------------|
| 1 | +5 Vdc Line Power |
| 2 | Data- |
| 3 | Data+ |
| 4 | Signal Gnd |
| 5 | Frame Gnd |
| 6 | Frame Gnd |

Table 8-3: USB Type B Connector Assignment

8.3 Ethernet

| Pin | Definition |
|-----|------------|
| 1 | Data A+ |
| 2 | Data A- |
| 3 | Data B+ |
| 4 | Data B- |
| 5 | Data C+ |
| 6 | Data C- |
| 7 | Data D+ |
| 8 | Data D- |

Table 8-4: Ethernet RJ-45 Connector Assignment

9.0 Power Requirements

The two AvBus expansion connectors provide power for the circuits on the Expansion card. All devices on the expansion card operate at +3.3 volts. A National Semiconductor LP3966ES-1.8 LDO (U21) is used to generate the 1.8 volt core voltage supply for the Ethernet PHY. Input current requirements are TBD. Two LEDs indicate input power on the +3.3V (D9) and +5V (D10) power rails.